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| ART UNIT | PAPER NUMBER |
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| 2111 | |

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/866,005 | SCHMISSEUR ET AL. | |
| | Examiner | Art Unit | |
| | Thomas J. Cleary | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). *Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any* earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4, 5, 6, 9, 10, 12, 13, 14, 21, 22, 24, 26, 27, and 29 are rejected under 35 U.S.C. 102(a) as being anticipated by 6,101,557 to Movall et al. ("Movall").

3. In reference to Claim 1, Movall discloses a system comprising: a peripheral device (See Figure 2B Number 260) adapted to define a plurality of device functions (See Figure 2B Numbers 250-0 – 250-N) accessible through a data interface (See Figure 2B Number 400) with a data bus (See Figure 2A Number 300); a first processing system adapted to communicate with a first device function defined by the peripheral device through the data interface (See Figure 2B Number 250-0 and Column 6 Lines 35-44); and a second processing system adapted to communicate with a second function defined by the peripheral device through the data interface (See Figure 2A Number 100 and Column 6 Lines 35-44).

4. In reference to Claim 2, Movall discloses the limitations as applied to Claim 1 above. Movall further discloses that each device is an I/O device (See Figure 3 Number 280-N and Column 5 Lines 4-19), and therefore the first processing system comprises logic to enumerate each device function associated with an I/O channel (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58).

5. In reference to Claim 4, Movall discloses the limitations as applied to Claim 1 above. Movall further discloses that the second processing system is coupled to the data bus through a bridge (See Figure 1B Number 210 and Column 4 Line 59 – Column 5 Line 3) and the first processing system is a peripheral device (See Figure 2B Number 250-0).

6. In reference to Claim 5, Movall discloses the limitations as applied to Claim 1 above. Movall further discloses that the first processing system comprises logic to cause the peripheral device to conceal one or more device functions from the second processing system while enabling the second processing system to communicate with at least one unconcealed device function defined by the peripheral device (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

7. In reference to Claim 6, Movall discloses the limitations as applied to Claim 5 above. Movall further discloses that the first processing system comprises: logic to enumerate a first device function defined by the peripheral device (See Figures 3 and 4

and Column 6 Line 51 – Column 8 Line 58); and logic to set information in a configuration header maintained at the peripheral device to conceal one or more device functions from the second processing system (See Column 6 Lines 25-44 and Column 8 Lines 37-43) while enabling the first processing system to communicate with the first device function (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

8. In reference to Claim 9, Movall discloses a method comprising: initiating a first enumeration procedure at a first processing system (See Figure 2B Number 250-0) to enumerate a first device function defined by a peripheral device (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58) coupled to a data interface (See Figure 2B Number 400) of a data bus (See Figure 2A Number 300); and initiating a second enumeration procedure at a second processing system to enumerate a second device function defined by the peripheral device (See Column 8 Lines 59-63).

9. In reference to Claim 10, Movall discloses the limitations as applied to Claim 9 above. Movall further discloses that each device is an I/O device (See Figure 3 Number 280-N and Column 5 Lines 4-19), and therefore the method further comprises enumerating at least one device function associated with an I/O channel (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58).

10. In reference to Claim 12, Movall discloses the limitations as applied to Claim 9 above. Movall further discloses that the second processing system is coupled to the

data bus through a bridge (See Figure 1B Number 210 and Column 4 Line 59 – Column 5 Line 3) and the first processing system is a peripheral device (See Figure 2B Number 250-0).

11. In reference to Claim 13, Movall discloses the limitations as applied to Claim 9 above. Movall further discloses causing the peripheral device to conceal one or more device functions from the second processing system while enabling the second processing system to communicate with at least one unconcealed device function defined by the peripheral device (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

12. In reference to Claim 14, Movall discloses the limitations as applied to Claim 13 above. Movall further discloses that the method further comprises: enumerating a first device function defined by the peripheral device (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58); and setting information in a configuration header maintained at the peripheral device to conceal the first device function from the second processing system (See Column 6 Lines 25-44 and Column 8 Lines 37-43) while enabling the first processing system to communicate with the first device function (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

13. In reference to Claim 21, Movall discloses a processing system comprising: logic to initiate a first enumeration procedure to enumerate a first device function defined by a

peripheral device (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58) coupled to a data interface (See Figure 2B Number 400) of a data bus (See Figure 2A Number 300); and logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures (See Column 6 Lines 40-44).

14. In reference to Claim 22, Movall discloses the limitations as applied to Claim 21 above. Movall further discloses that each device is an I/O device (See Figure 3 Number 280-N and Column 5 Lines 4-19), and therefore the processing system further comprises logic to enumerate the first device function as an I/O channel (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58).

15. In reference to Claim 24, Movall discloses the limitations as applied to Claim 21 above. Movall further discloses that the processing system comprises: logic to initiate a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures (See Column 6 Lines 25-44 and Column 8 Lines 37-43) while enabling the first processing system to communicate with the first device function (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

16. In reference to Claim 26, Movall discloses a method comprising: initiating a first enumeration procedure at a first processing system (See Figure 2B Number 250-0) to

enumerate a first device function defined by a peripheral device (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58) coupled to a data interface (See Figure 2B Number 400) of a data bus (See Figure 2A Number 300); and initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures (See Column 6 Lines 40-44) while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

17. In reference to Claim 27, Movall discloses the limitations as applied to Claim 26 above. Movall further discloses that each device is an I/O device (See Figure 3 Number 280-N and Column 5 Lines 4-19), and therefore the method further comprises enumerating the first device function as an I/O channel (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58).

18. In reference to Claim 29, Movall discloses the limitations as applied to Claim 26 above. Movall further discloses that the method further comprises: initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures (See Column 6 Lines 25-44 and Column 8 Lines 37-43) while enabling the first processing system to communicate with the first device function (See Column 6 Lines 40-44 and Column 8 Lines 59-63).

19. Claims 1, 2, 4, 5, 9, 10, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by US Patent Number 6,212,587 to Emerson et al. ("Emerson").

20. In reference to Claim 1, Emerson discloses a system comprising: a peripheral device (See Figure 1 Number 200 and Figure 4 Item V) adapted to define a plurality of device functions accessible through a data interface (See Figure 1 Number 230 and Figure 4 Item II) with a data bus; a first processing system (See Figure 1 Number 290, Column 4 Lines 18-64, and Figure 4 Item III) adapted to communicate with a first device function defined by the peripheral device through the data interface (See Figure 1 Number 270, Column 4 Lines 18-64, and Figure 4 Item I); and a second processing system (See Figure 1 Number 250, Column 4 Lines 6-17, and Figure 4 Item I) adapted to communicate with a second device function defined by the peripheral device through the data interface (See Figure 1 Number 240, Column 4 Lines 6-17, and Figure 4 Item VI). For clarity, Figure 4 of Emerson has been reproduced below with annotations.

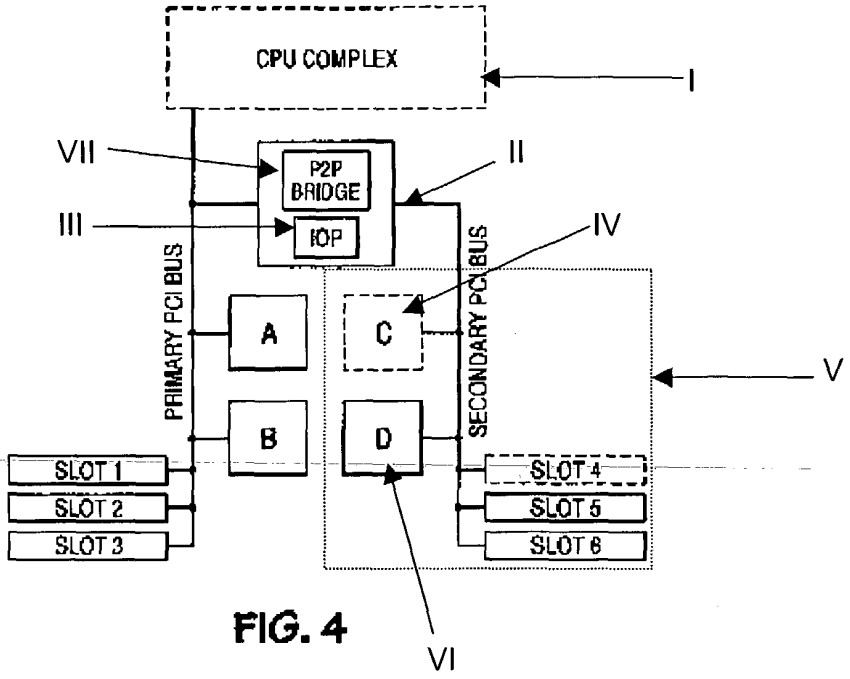


FIG. 4

21. In reference to Claim 2, Emerson teaches the limitations as applied to Claim 1 above. Emerson further teaches that the devices are I/O devices (See Column 4 Lines 20-23), and thus each device that is enumerated by the first processor is enumerated as an I/O channel.

22. In reference to Claim 4, Emerson discloses the limitations as applied to Claim 1 above. Emerson further discloses that the second processing system is coupled to the data bus through a bridge (See Figure 1 Number 210 and Figure 4 Item VII) and the first processing system is a peripheral device (See Figure 1 Number 290 and Figure 4 Item III).

23. In reference to Claim 5, Emerson discloses the limitations as applied to Claim 1 above. Emerson further discloses that the first processing system comprises logic to conceal one or more device functions from the second processing system (See Column 4 Lines 30-44); and that both the hidden and non-hidden functions are on the same section of bus, which therefore enables the second processing system to communicate with the unconcealed functions while the remaining functions remain hidden (See Figure 1 and Column 4 Lines 15-17).

24. In reference to Claim 9, Emerson discloses a method comprising: initiating a first enumeration procedure at a first processing system to enumerate a first device function defined by a peripheral device coupled to a data interface of a data bus (See Column 3 Lines 10-17 and Column 4 Lines 18-64); and initiating a second enumeration procedure at a second processing system to enumerate a second device function defined by the peripheral device (See Column 3 Lines 10-17 and Column 4 Lines 6-17).

25. In reference to Claim 10, Emerson teaches the limitations as applied to Claim 9 above. Emerson further teaches that the devices are I/O devices (See Column 4 Lines 20-23), and thus each device that is enumerated is enumerated as an I/O channel.

26. In reference to Claim 12, Emerson discloses the limitations as applied to Claim 9 above. Emerson further discloses that the second processing system is coupled to the data bus through a bridge (See Figure 1 Number 210 and Figure 4 Item VII) and the first

processing system is a peripheral device (See Figure 1 Number 290 and Figure 4 Item III).

27. In reference to Claim 13, Emerson discloses the limitations as applied to Claim 9 above. Emerson further discloses causing the peripheral device to conceal one or more device functions from the second processing system (See Column 4 Lines 30-44); and that both the hidden and non-hidden functions are on the same section of bus, which therefore enables the second processing system to communicate with the unconcealed functions while the remaining functions remain hidden (See Figure 1 and Column 4 Lines 15-17).

***Claim Rejections - 35 USC § 103***

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 3, 11, 23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Movall as applied to Claims 2, 10, 22, and 27 above, and further in view of US Patent Number 6,044,207 to Pecone et al. ("Pecone").

30. In reference to Claim 3, Movall teaches the limitations as applied to Claim 2 above. Movall does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the peripheral RAID device of Pecone, resulting in the invention of Claim 3, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

31. In reference to Claim 11, Movall teaches the limitations as applied to Claim 10 above. Movall does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the peripheral RAID device of Pecone, resulting in the invention of Claim 11, in order to provide the ability to connect a

high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

32. In reference to Claim 23, Movall teaches the limitations as applied to Claim 22 above. Movall does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the peripheral RAID device of Pecone, resulting in the invention of Claim 23, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

33. In reference to Claim 28, Movall teaches the limitations as applied to Claim 27 above. Movall does not teach that the device function associated with the I/O channel

comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the peripheral RAID device of Pecone, resulting in the invention of Claim 28, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

34. Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Movall as applied to Claims 5 and 13 above, and further in view of US Patent Number 5,734,847 to Garbus et al. ("Garbus").

35. In reference to Claim 7, Movall teaches the limitations as applied to Claim 5 above. Movall does not teach that the bridge comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Garbus teaches a bridge that comprises logic to initiate execution of an enumeration process by the first processing

system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the enumeration logic and procedure of Garbus, resulting in the invention of Claim 7, in order to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

36. In reference to Claim 8, Movall teaches the limitations as applied to Claim 5 above. Movall does not teach that the first processing system comprises logic to transmit a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches that the first processing system transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 8, in order allow the hidden functions to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

37. In reference to Claim 15, Movall teaches the limitations as applied to Claim 13 above. Movall does not teach initiating execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Garbus teaches a bridge that comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the enumeration logic and procedure of Garbus, resulting in the invention of Claim 15, in order to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

38. In reference to Claim 16, Movall teaches the limitations as applied to Claim 13 above. Movall does not teach transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches that the first processing system transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 16, in order allow the

hidden functions to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

39. Claims 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Movall and US Patent Number 5,737,344 to Belser et al. ("Belser").

40. In reference to Claim 17, Movall teaches initiating a first enumeration procedure at a first processing system (See Figure 2B Number 250-0) to enumerate a first device function defined by a peripheral device (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58) coupled to a data interface (See Figure 2B Number 400) of a data bus (See Figure 2A Number 300); and initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures (See Column 6 Lines 40-44) while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Column 6 Lines 40-44 and Column 8 Lines 59-63). Movall does not teach a storage medium comprising machine-readable instructions. Belser teaches a processor that executes machine-readable instructions stored on a direct access storage device (See Column 4 Lines 5-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the storage medium

comprising machine-readable instructions of Belser, resulting in the invention of Claim 17, in order to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

41. In reference to Claim 18, Movall and Belser teach the limitations as applied to Claim 17 above. Movall further discloses that each device is an I/O device (See Figure 3 Number 280-N and Column 5 Lines 4-19), and therefore further comprises enumerating the first device function as an I/O channel (See Figures 3 and 4 and Column 6 Line 51 – Column 8 Line 58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 18, in order to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

42. In reference to Claim 20, Movall discloses the limitations as applied to Claim 17 above. Movall further teaches: initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures (See Column 6 Lines 25-44 and Column 8 Lines 37-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the storage medium

comprising machine-readable instructions of Belser, resulting in the invention of Claim 20, in order to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

43. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Movall as applied to Claim 17 above, and further in view of Pecone.

44. In reference to Claim 19, Movall teaches the limitations as applied to Claim 17 above. Movall does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Movall with the peripheral RAID device of Pecone, resulting in the invention of Claim 19, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

45. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Movall as applied to Claim 24 above, and further in view of US Patent Number 5,960,213 to Wilson ("Wilson").

46. In reference to Claim 25, Movall teaches the limitations as applied to Claim 24 above. Movall does not teach that the processing system further comprising logic to initiate a bus transaction to modify data in a Header Type register of the configuration header. Wilson teaches a unit that sends signals to set a bit in the Header Type register of the devices connected to it (See Column 6 Lines 21-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Movall with the device to set the Header Type register of Wilson, resulting in the invention of Claim 25, in order to allow the host system to view the secondary PCI devices as a single multifunction device (See Column 6 Lines 7-10 of Wilson).

47. Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson as applied to Claim 2 above, and further in view of Pecone.

48. In reference to Claim 3, Emerson teaches the limitations as applied to Claim 2 above. Emerson does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the

devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson with the peripheral RAID device of Pecone, resulting in the invention of Claim 3, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

49. In reference to Claim 11, Emerson teaches the limitations as applied to Claim 10 above. Emerson does not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson with the peripheral RAID device of Pecone, resulting in the invention of Claim 11, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available

data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

50. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson as applied to Claims 5 above, and further in view of US Patent Number 6,678,770 to Sutoh ("Sutoh").

51. In reference to Claim 6, Emerson teaches the limitations as applied to Claim 5 above. Emerson further teaches that the first processing system comprises logic to enumerate a first device function of the peripheral device (See Column 3 Lines 10-17 and Column 4 Lines 18-64). Emerson does not teach that the first processing system comprises logic to set information in a configuration header maintained at the peripheral device to conceal the first function from the second processing system while enabling the first processing system to communicate with the first device function. Sutoh teaches setting information in a device to indicate whether the master device controls it or whether another device on the bus controls it, thus concealing it from the master device (See Abstract, Column 1 Line 59 – Column 2 Line 15, and Column 6 Lines 50-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the ability to set device owners of Sutoh, resulting in the invention of Claim 6, in order to enable services provided by non-intelligent devices to be initialized and managed by intelligent devices (See Column 1 Lines 43-45 of Sutoh).

52. In reference to Claim 14, Emerson teaches the limitations as applied to Claim 13 above. Emerson further teaches enumerating a first device function of the peripheral device (See Column 3 Lines 10-17 and Column 4 Lines 18-64). Emerson does not teach setting information in a configuration header maintained at the peripheral device to conceal the first device function from the second processing system while enabling the first processing system to communicate with the first device function. Sutoh teaches setting information in a device to indicate whether the master device controls it or whether another device on the bus controls it, thus concealing it from the master device (See Abstract, Column 1 Line 59 – Column 2 Line 15, and Column 6 Lines 50-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the ability to set device owners of Sutoh, resulting in the invention of Claim 14, in order to enable services provided by non-intelligent devices to be initialized and managed by intelligent devices (See Column 1 Lines 43-45 of Sutoh).

53. Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson as applied to Claims 5 and 13 above, and further in view of Garbus.

54. In reference to Claim 7, Emerson teaches the limitations as applied to Claim 5 above. Emerson further teaches a bridge coupled to the peripheral device through a

secondary bus (See Figure 1 Number 210). Emerson does not teach that the bridge comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Garbus teaches a bridge that comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson with the enumeration logic and procedure of Garbus, resulting in the invention of Claim 7, in order to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

55. In reference to Claim 8, Emerson teaches the limitations as applied to Claim 5 above. Emerson does not teach that the first processing system comprises logic to transmit a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches that the first processing system transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 8, in

order allow the hidden functions to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

56. In reference to Claim 15, Emerson teaches the limitations as applied to Claim 13 above. Emerson does not teach initiating execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Garbus teaches a bridge that comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson with the enumeration logic and procedure of Garbus, resulting in the invention of Claim 15, in order to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

57. In reference to Claim 16, Emerson teaches the limitations as applied to Claim 13 above. Emerson does not teach transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches that the first processing system transmitting a signal to the peripheral device to

inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 16, in order allow the hidden functions to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to functions that are to be hidden (See Column 2 Lines 18-21 of Garbus).

58. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson, Garbus, and Belser.

59. In reference to Claim 17, Emerson teaches initiating a first enumeration procedure (See Column 3 Lines 10-17) at a first processing system (See Figure 1 Number 290, Column 4 Lines 18-64, and Figure 4 Item III) to enumerate a first device function defined by a peripheral device (See Figure 1 Number 200 and Figure 4 Item V) coupled to a data interface (See Figure 1 Number 230 and Figure 4 Item II) of a data bus; the peripheral device defining a plurality of device functions (See Figure 1 Number 200 and Figure 4 Item V). Emerson does not teach initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the

peripheral device to be enumerated by a subsequent enumeration procedure; and a storage medium comprising machine-readable instructions. Garbus teaches initiating a bus transaction on the data bus to cause the first element to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57). Belser teaches a processor that executes machine-readable instructions stored on a direct access storage device (See Column 4 Lines 5-15). For clarity, Figure 4 of Emerson has been reproduced with annotations below the rejection of Claim 1 above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus and the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 17, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus); and to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

60. In reference to Claim 18, Emerson, Garbus, and Belser teach the limitations as applied to Claim 17 above. Emerson further teaches that the devices are I/O devices (See Column 4 Lines 20-23), and thus each device that is enumerated is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus and the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 18, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus); and to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

61. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson, Garbus, and Belser as applied to Claim 18 above, and further in view of Pecone.

62. In reference to Claim 19, Emerson, Garbus, and Belser teach the limitations as applied to Claim 18 above. Emerson, Garbus, and Belser do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson, Garbus, and Belser with the peripheral RAID device of Pecone, resulting in the invention of Claim 19, in order to provide the ability to connect a high performance external storage system that allows for

managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

63. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson, Garbus, and Belser as applied to Claim 17 above, and further in view of US Patent Number 6,647,434 to Kamepalli ("Kamepalli").

64. In reference to Claim 20, Emerson, Garbus, and Belser teach the limitations as applied to Claim 17 above. Emerson, Garbus, and Belser do not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can communicate with the CPU or disabled and cannot communicate with or be enumerated by the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson, Garbus, and Belser with the device header system of Kamepalli, resulting in the invention of Claim 20, in order to allow a hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

65. Claims 21, 22, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson and Garbus.

66. In reference to Claim 21, Emerson teaches logic to initiate a first enumeration procedure (See Column 3 Lines 10-17) to enumerate a first device function defined by a peripheral device (See Figure 1 Number 200 and Figure 4 Item V) coupled to a data interface (See Figure 1 Number 230 and Figure 4 Item II) of a data bus; the peripheral device defining a plurality of device functions (See Figure 1 Number 200 and Figure 4 Item V). Emerson does not teach logic to initiate a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedure to access at least one other device function defined by the peripheral device. Garbus teaches initiating a bus transaction on the data bus to cause the first element to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57). For clarity, Figure 4 of Emerson has been reproduced with annotations below the rejection of Claim 1 above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus, resulting in the invention of Claim 21, in order to prevent the host processor

from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

67. In reference to Claim 22, Emerson and Garbus teach the limitations as applied to Claim 21 above. Emerson further teaches that the devices are I/O devices (See Column 4 Lines 20-23), and thus each device that is enumerated is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus, resulting in the invention of Claim 22, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

68. In reference to Claim 26, Emerson teaches initiating a first enumeration procedure (See Column 3 Lines 10-17) at a first processing system (See Figure 1 Number 290, Column 4 Lines 18-64, and Figure 4 Item III) to enumerate a first device function defined by a peripheral device (See Figure 1 Number 200 and Figure 4 Item V) coupled to a data interface (See Figure 1 Number 230 and Figure 4 Item II) of a data bus; the peripheral device defining a plurality of device functions (See Figure 1 Number 200 and Figure 4 Item V). Emerson does not teach initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the

peripheral device to be enumerated by a subsequent enumeration procedure. Garbus teaches initiating a bus transaction on the data bus to cause the first element to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57). For clarity, Figure 4 of Emerson has been reproduced with annotations below the rejection of Claim 1 above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus, resulting in the invention of Claim 26, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

69. In reference to Claim 27, Emerson and Garbus teach the limitations as applied to Claim 26 above. Emerson further teaches that the devices are I/O devices (See Column 4 Lines 20-23), and thus each device that is enumerated is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson with the enumeration procedure of Garbus and the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 27, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See

Column 2 Lines 18-21 of Garbus); and to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

70. Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson and Garbus as applied to Claims 22 and 27above, and further in view of Pecone.

71. In reference to Claim 23, Emerson and Garbus teach the limitations as applied to Claim 22 above. Emerson and Garbus do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson and Garbus with the peripheral RAID device of Pecone, resulting in the invention of Claim 23, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

72. In reference to Claim 28, Emerson and Garbus teach the limitations as applied to Claim 27 above. Emerson and Garbus do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Emerson and Garbus with the peripheral RAID device of Pecone, resulting in the invention of Claim 28, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

73. Claims 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson and Garbus as applied to Claims 21 and 26 above, and further in view of Sutoh.

74. In reference to Claim 24, Emerson and Garbus teach the limitations as applied to Claim 21 above. Emerson does not teach that the first processing system comprises logic to initiate a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent

enumeration procedures while enabling the processing system to communicate with the first device function. Sutoh teaches setting information in a device to indicate whether the master device controls it or whether another device on the bus controls it, thus concealing it from the master device (See Abstract, Column 1 Line 59 – Column 2 Line 15, and Column 6 Lines 50-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson and Garbus with the ability to set device owners of Sutoh, resulting in the invention of Claim 24, in order to enable services provided by non-intelligent devices to be initialized and managed by intelligent devices (See Column 1 Lines 43-45 of Sutoh).

75. In reference to Claim 29, Emerson and Garbus teach the limitations as applied to Claim 26 above. Emerson does not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures while enabling the processing system to communicate with the first device function. Sutoh teaches setting information in a device to indicate whether the master device controls it or whether another device on the bus controls it, thus concealing it from the master device (See Abstract, Column 1 Line 59 – Column 2 Line 15, and Column 6 Lines 50-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson and Garbus with the ability to set device owners of Sutoh, resulting in the invention of Claim 29, in order to enable

services provided by non-intelligent devices to be initialized and managed by intelligent devices (See Column 1 Lines 43-45 of Sutoh).

76. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson, Garbus, and Kamepalli as applied to Claim 24 above, and further in view of Wilson.

77. In reference to Claim 25, Emerson, Garbus, and Kamepalli teach the limitations as applied to Claim 24 above. Emerson, Garbus, and Kamepalli do not teach that the processing system further comprising logic to initiate a bus transaction to modify data in a Header Type register of the configuration header. Wilson teaches a unit that sends signals to set a bit in the Header Type register of the devices connected to it (See Column 6 Lines 21-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Emerson, Garbus, and Kamepalli with the device to set the Header Type of Wilson, resulting in the invention of Claim 25, in order to allow the host system to view the secondary PCI devices as a single multifunction device (See Column 6 Lines 7-10 of Wilson).

***Drawings***

78. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the bridge of Claims 4, 7, and 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Response to Arguments*

79. Applicant's arguments, see Pages 10-14, filed 14 June 2004, with respect to the rejection(s)of claim(s) 1-29 under 35 USC §§ 102 and 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art and a different interpretation of previously applied references, as shown above.

### *Information Disclosure Statement*

80. An information disclosure statement is listed in the current application as having been filed on 9 August 2004. However, no copy of this IDS is present in the file. Applicant is advised to resubmit a copy of this IDS to be considered by the Examiner.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Beginning November 2004, the Examiner's telephone number will be changing to 571-272-3624, and the Examiner's supervisor's telephone number will be changing to 571-272-3632.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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